1213.43667X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Hirofumi SAHARA et al.

Serial No.: 10/802,859

Filed: March 18, 2004

For: INFORMATION PROCESSING SYSTEM AND METHOD

PETITION TO MAKE SPECIAL
UNDER 37 CFR 1.102(d) and MPEP. §708.02, VIII

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 4, 2005

Sir:

1. Petition

Applicants hereby petition to make this application **Special**, in accordance with 37 CFR §1.102(d) and MPEP 708.02, VIII. The present invention is a new application filed in the United States Patent and Trademark Office on March 18, 2004 and as such has not received any examination by the Examiner.

2. Claims

Applicants hereby represent that all the claims in the present application are directed to a single invention. If upon examination it is determined that all the claims presented are not directed to a single invention, Applicants will make an election without traverse as a prerequisite to the granting of special status.

01/05/2005 JBALINAN 00000008 10802859
01 FC:1464 130.00 OP

3. Search

Applicants hereby submit that a pre-examination search has been made by a professional searcher, (a copy of which is attached), in the following classes and subclasses:

Class	Subclass
711	118, 137, 213
714	2, 4, 8

4. Copy of References

A listing of all references found by the professional searcher has already been provided on a Form PTO-1449 and copies of the references and the Form PTO-1449 were submitted as part of an Information Disclosure Statement (IDS) previously filed on October 6, 2004.

5. Detailed Discussion of the References and Distinctions Between the References and the Claims

Below is a discussion of the references uncovered by the search and cited in the IDS filed on even date that appear to be most closely related to the subject matter encompassed by the claims of the present application, and which discussion particularly points out how Applicants' claimed subject matter is distinguishable over those references. All other references uncovered by the search and cited in the IDS filed on even date are **not** treated in detail herein.

a. Detailed Discussion of the References

U.S. Patent No. 5,740,465 (Matsunami et al.), assigned to Hitachi, Ltd., is entitled Array Disk Controller for Grouping Host Commands into a Single Virtual Host

Command. Disclosed is a plurality of commands that can be sent sequentially from a host computer 1 and are interpreted by a host command interpreter 13 to generate a disk command for each disk unit 9a, 9b, 9e. A selection condition is detected from the I/O demand information supplied by a host computer, and an optimum one of a plurality of RMW processing systems is selected and executed on the basis of the selection condition. A prefetch controller 19 that is installed in command controller 6 generates a disk command to read data in the logical address area following the access area of the host command A of the disk units 9c, 9d, and sends the disk command to the disk command start/end means 15. The read demand that has been sent to the disk units 9c, 9d is stored in prefetch controller 19 (see figures 1, 2, 15, and 16; abstract; and column 19, lines 10-17).

U.S. Patent No. 5,940,838 (Schmuck et al.), assigned to International Business Machines Corp., is entitled Parallel File System and Method Anticipating Cache Usage Patterns. Disclosed is prefetching, which is a technique used in file systems to reduce I/O latency by reading blocks of sequentially accessed files in advance of when the data is requested by application programs, in a parallel file system. Within the system is a system service called the "buffer manager", which arbitrates use of memory resources among different system components competing for memory. The buffer manager is provided with appropriate information to take into account resources required for prefetching. A file system buffer pool is logically divided into two parts, one used for prefetching and one used for caching recently accessed file blocks. These pools are presented to the buffer manager as two separate components (see figure 2; and column 20, lines 12-15, 18-23, 40-41, 48-50, and 57-58). Note: U.S. patent

6,021,508 is similar.

U.S. Patent No. 2003/0163649 A1 (Kapur et al.) is entitled Shared Bypass Bus Structure. Disclosed is a pre-fetch engine 286 located in I/O hubs/bridges that is responsible for handling the read requests from the peripheral I/O devices or I/O bridges and pre-fetching ahead of these requests from the system memory to provide high streaming bandwidth. A unified cache can comprise adaptive pre-fetch scheduling to use a unified common read cache/buffer of size XYZ-KB across more than one stream, or restrict the maximum total cache/buffer usage across the more than one stream to the unified cache/buffer size of XYZ-KB wherein XYZ can be larger than the amount of useful pre-fetch data for continuous streaming to smoothly transition between different numbers of streams, or restrict the maximum cache/buffer usage per stream by using a look-up table that uses N to look up a pre-set table to determine the maximum allowed cache/buffer usage per stream for that N or by using a formula that is computed for a given N (see figures 9, 12;and paragraphs 125and 127). Note: U.S. Patent applications 2003/0177320 A1 and 2004/0022094 A1 are similar and are included for reference.

b. Distinctions Between the References and the Claims

The present invention as recited in the claims filed are not taught or suggested by any of the above noted references whether taken individually or in combination with each other or in combination with any of the other references now of record.

The present invention as recited in the claims is directed to an information processing system that includes storage equipment which includes a logical unit

logically assigned to physical devices and an information processing apparatus which sends data I/O requests to the storage equipment. The data I/O requests are transferred through logical paths serving as communication paths to the logical unit, and a cache memory is provided to prefetch and store both data in a location to be accessed by one of the data I/O requests and data in locations following the location within the physical devices. The information processing apparatus includes a path selection management section which manages configurations of a plurality of blocks into which the logical unit is divided, an I/O request allocation section which allocates data I/O requests to be transmitted to the storage equipment to the logical paths, and I/O processing units which transmit data I/O requests through the logical paths, according to the allocation determined by the I/O request allocation section, pursuant to an established protocol, where the path selection management section assigns at least one of the logical paths to one of the blocks.

The above described features of the present invention, particularly path selection management that manages configurations of a plurality of blocks into which the logical unit is divided, I/O request allocation that allocates data I/O requests to be transmitted to the storage equipment to the logical paths, or I/O processing that transmits data I/O requests through the logical paths, according to the allocation determined by the I/O request allocation section, or a path management table, an LU management table, a block management table, or selecting, based on one data input/output request, an I/O processing unit assigned to a block where data to be accessed by the data input/output request exists and making the selected I/O processing unit process the data input/output request, or selecting an I/O processing unit that processed the last data input/output request

and making the cache memory work, if the data to be accessed by the data input/output request is not stored on the cache memory, or selecting an I/O processing unit assigned to a block where the data to be accessed by the data input/output request exists and making the selected I/O processing unit process the data input/output request, are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

6. Fee (37 C.F.R. 1.17(i))

The fee required by 37 C.F.R. § 1.17(i) is to be paid by:

[X] the Credit Card Payment Form (attached) for $130.00.

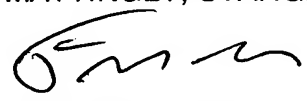
[ ] charging Account _____ the sum of $130.00.

A duplicate of this petition is attached.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger & Malur, Deposit Account No. 50-1417 (1213.43667x00).

Respectfully submitted,

MATTINGLY, STANGER & MALUR, P.C.



Frederick D. Bailey
Registration No. 42,282

FDB/sdb
Enclosures

COPY

1213.43667X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): H. SAHARA, et al

Serial No.: 10/802,859

Filed: March 18, 2004

For: INFORMATION PROCESSING SYSTEM AND METHOD

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97 & 1.98

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

October 6, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (1213.43667X00) please credit any excess fees to such deposit account.

Respectfully submitted,

Carl I. Brundidge
Registration No. 29,621
ANTONELLI, TERRY, STOUT & KRAUS, LLP

CIB/jdc
(703) 312-6600

FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
1213.43667X00	10/802,859
APPLICANT: H. SAHARA, et al	
FILING DATE: March 18, 2004	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,744,046	4/98	Matsunami et al			
		5,940,838	8/99	Schmuck et al			
		6,021,508	2/00	Schmuck et al			
	2003	0,163,649	8/03	Kapur et al			
	2003	0,177,320	9/03	Sah et al			
	2004	0,022,094	2/04	Radhakrishnan et al			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT YES	ABSTRACT NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

(Form PTO-1449 [6-4])

October 28, 2004

Via Federal Express
Noboru Otsuka
Hitachi, Ltd.
IP Development & Management Division
Patent Dept. 4
292, Yoshida-cho, Totsuka, Yokohama-shi

Kanagawa, Japan 244-0817

RE: PATENTABILITY SEARCH FOR INFORMATION PROCESSING SYSTEM AND METHOD
Your File: 340301107US01
Our Docket: PSP-1041788

Dear Mr. Otsuka:

In accordance with your request, we have conducted a patentability search on the above-identified subject matter.

Enclosed with this report are copies of the search results and your disclosure materials. If after reviewing the results, you feel that the search feature (or specific search elements), the field of search, or results are not commensurate with your original request, or you would like to extend the search into additional areas, please contact us.

Sincerely,

Randy W. Lacasse

Enclosures
RWL:SG:dcw
s04/psp1041788

CONFIDENTIAL
(Patentability Search)

I. SEARCH FEATURE

A. General

Information processing system

B. Specific

An information processing system that includes storage equipment which includes a logical unit assigned to physical devices and an information processing apparatus which sends data I/O requests to the storage equipment. The data I/O requests are transferred through logical paths serving as communication paths to the logical unit, and a cache memory is provided to prefetch and store both data in a location to be accessed by one of the data I/O requests and data in locations following the location within said physical devices. The information processing apparatus comprises a path selection management section which manages configurations of a plurality of blocks into which a logical unit is divided, and a I/O request allocation section which allocates data I/O requests to be transmitted to storage equipment to logical paths, and I/O processing units which transmit data I/O requests through logical paths, according to the allocation determined by I/O request allocation section, where the path selection management section assigns at least one logical path to one block.

C. Application

Memory storage accessing and control in a storage system

II. FIELD OF SEARCH

The search of the above features was conducted in the following areas:

A. Classification search

Class	Subclasses	Description
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**
	118	..Caching
	137	...Look-ahead
	213	Generating prefetch, look-ahead, jump, or predictive address

Class	Subclasses	Description (continued)
714/		**ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY**
	2	..Fault recovery
	4	....Of network
	8	....Isolating failed storage location (e.g., sector remapping)

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). No further integrity studies were performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

III. RESULTS OF SEARCH

A. References developed as a result of search:

U.S. Patent No.	Inventor
*5,740,465	Matsunami et al.
5,940,838	Schmuck et al.
6,021,508	Schmuck et al.

U.S. Patent Application Publication No.	Inventor
2003/0163649 A1	Kapur et al.
2003/0177320 A1	Sah et al.
2004/0022094 A1	Radhakrishnan et al.

**Relevant patents/applications assigned to Hitachi, Ltd.*

B. Discussion of related references in numerical order:

The patent to Matsunami et al. (5,740,465), assigned to Hitachi, Ltd., provides for an *Array Disk Controller for Grouping Host Commands into a Single Virtual Host Command.* Discussed is a plurality of commands that can be sent sequentially from a host computer **1** and are interpreted by a host command interpreter **13** to generate a disk command for each disk unit **9a, 9b, 9e.** A selection condition is detected from the I/O demand information supplied by a host computer, and an optimum one of a plurality of RMW processing systems is selected and executed on the basis of the selection condition. A prefetch controller **19** that is installed in command controller **6** generates a disk command to read

data in the logical address area following the access area of the host command A of the disk units **9c**, **9d**, and sends the disk command to the disk command start/end means **15**. The read demand that has been sent to the disk units **9c**, **9d** is stored in prefetch controller **19** (see figures 1, 2, 15, and 16; abstract; and column 19, lines 10-17).

The patent to Schmuck et al. (5,940,838), assigned to International Business Machines Corp., provides for a *Parallel File System and Method Anticipating Cache Usage Patterns*. Discussed is prefetching, which is a technique used in file systems to reduce I/O latency by reading blocks of sequentially accessed files in advance of when the data is requested by application programs, in a parallel file system. Within the system is a system service called the "buffer manager", which arbitrates use of memory resources among different system components competing for memory. The buffer manager is provided with appropriate information to take into account resources required for prefetching. A file system buffer pool is logically divided into two parts, one used for prefetching and one used for caching recently accessed file blocks. These pools are presented to the buffer manager as two separate components (see figure 2; and column 20, lines 12-15, 18-23, 40-41, 48-50, and 57-58). Note: U.S. patent 6,021,508 is similar.

The patent application to Kapur et al. (2003/0163649 A1) provides for a *Shared Bypass Bus Structure*. Disclosed is a pre-fetch engine 286 located in I/O hubs/bridges that is responsible for handling the read requests from the peripheral I/O devices or I/O bridges and pre-fetching ahead of these requests from the system memory to provide high streaming bandwidth. A unified cache can comprise adaptive pre-fetch scheduling to use a unified common read cache/buffer of size XYZ-KB across more than one stream, or restrict the maximum total cache/buffer usage across the more than one stream to the unified cache/buffer size of XYZ-KB wherein XYZ can be larger than the amount of useful pre-fetch data for continuous streaming to smoothly transition between different numbers of streams, or restrict the maximum cache/buffer usage per stream by using a look-up table that uses N to look up a pre-set table to determine the maximum allowed cache/buffer usage per stream for that N or by using a formula that is computed for a given N (see figures 9, 12;and paragraphs 125and 127). Note: U.S. Patent applications 2003/0177320 A1 and 2004/0022094 A1 are similar and are included for reference.

Sejal Gangar